International Journal of Latest Trends in Engineering and Technology
Vol.(10)Issue(2), pp. 195-201
DOI: http://dx.doi.org/10.21172/1.102.32
e-ISSN:2278-621X

HYBRID MULTICARRIER MODULATION USING LOOKUP TABLE METHOD FOR REDUCTION OF LEAKAGE CURRENT IN CASCADED MULTILEVEL INVERTER

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Abstract- In this paper a novel technique is introduced for Cascaded Multilevel Inverter using Lookup Table Method for reduction of leakage current. The performance of the Hybrid Multicarrier Modulation using Lookup Table Method (HMCMLTM) and its effect on leakage current was analyzed with HMCM using Third Harmonic Injection (HMCMTHI) and HMCM (Without LTM and THI) in MATLAB/SIMULINK environment. It was inferred that the HMCMLTM possess lesser leakage current with higher fundamental voltage and lesser harmonics when compared with other existing techniques. The hardware setup is built for HMCMLTM and the inverter is operated by using microcontroller (ATMEGA328P-PU) controller which generates PWM pulses. The semiconductor switching device (MOSFET Driver IR2110) is used for the switching purpose to obtain the required output. And the hardware results are validated with the simulation results.
Keywords – Multilevel Inverter, Leakage Current, Common Mode Voltage, Pulse Width Modulation, Total Harmonics Distortion.

1. INTRODUCTION

Cascaded H-bridge (CHB) multilevel inverter has been widely applied in various high power applications since it requires less number of components for synthesizing the desired voltage level. Transformerless grid connected PV system improves the efficiency and makes the whole system lighter but it has safety issues due to high leakage current which is produced due to the large common mode voltage. The leakage current is due to the fact that when the inverter output voltage becomes zero, there is a flow of current between the PV system and grid, this is due to the internal parasitic capacitance of the PV system [1]-[2]. The magnitude of leakage current purely depends on the common mode voltage existing between each leg of the inverter and ground. This can be reduced by adopting suitable PWM techniques. HMCMLTM is one such technique which reduces leakage current to a great extent when compared to other hybrid techniques.

2. CASCADED MULTILEVEL INVERTER

A single phase cascaded multilevel inverter is shown in Fig. 1 . The output phase voltage level m in a cascade inverter is given by $m = 2s + 1$, where s is the number of separate dc sources. The stepped output voltage and current for various levels can be obtained by cascading several H-bridge inverters together. Each inverter can produce three distinct outputs, namely as +Vdc, 0, -Vdc by varying the switching sequence. Here I_L denotes the leakage current and V_{cm} represents the CMV. The CMV for the upper full H-bridge inverter is given in equation (1)

$$V_{cm} = \frac{V\alpha N + V\beta N}{2} \tag{1}$$

The CMV for cascaded multilevel inverter can be written as in equation (2)

$$V_{cm} = \frac{V_{\alpha'\beta'} - V_{\alpha N} - V_{\beta N}}{2} \tag{2}$$

The CMV is maintained at minimum during the switching instances to ensure reduction in the leakage current flowing through the parasitic capacitance. The characteristics of the leakage current and CMV are explained with the help of sinusoidal PWM techniques. Here the intersection of sine wave and triangle wave are used for generating the gate pulse [3]-[4].

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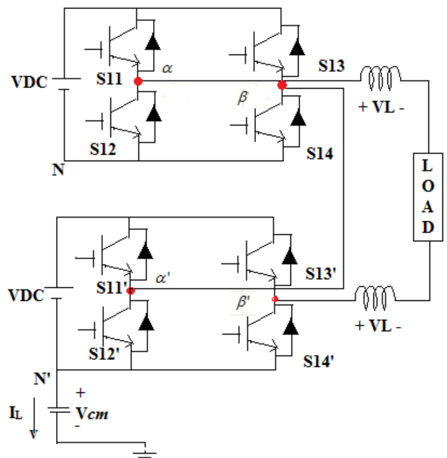

Figure 1. Two stage cascaded multilevel inverter

3. ARDUINO UNO

An Arduino board shown in Fig. 2 consists of an 8- bit Atmel AVR microcontroller with complementary components to facilitate programming and incorporating into other circuit. Arduino's have used the mega AVR series of chips, specially the Atmega 8, ATmegs168, ATmega328, ATmega1280 and ATmega2560. Most boards include a 5 volt linear regulator and 16MHZ crystal oscillator.

Figure 2. ARDUINO UNO

An Arduino's microcontroller is also pre-programmed with a boot loader that simplifies uploading of programs to the on-chip flash memory. Atmega328P-PU is used for the Cascaded Multilevel Inverter. Analog data from Matlab Simulink is fed to the microcontroller which produces digital gate pulses for the power circuit by interfacing Arduino software with Matlab Simulink environment [5].

4. HYBRID MULTICARRIER MODULATION (HMCM)

The HMCPWM is the modified version of the Phase Opposite Disposition (POD) pulse width modulation technique, where the number of carriers required is half of that required in POD PWM and therefore computational burden is reduced. In this modulation technique the phase of all the carriers are shifted by 180° after each half cycle. The HMCPWM carrier waveform is shown in Fig.3. It has six switching instants, in which one instant has zero CMV, three instants have 2VPV/4 and two instants have VPV/4, CMV. There is no voltage transition in zero CMV. The CMV may take the values depending upon the inverter switch states selected. The voltage transition depends upon the direction of the current in the inverter, hence the proposed H-MCPWM modulation technique reduces the common mode voltage generation in the band limit of maximum ± VPV/4 [6].

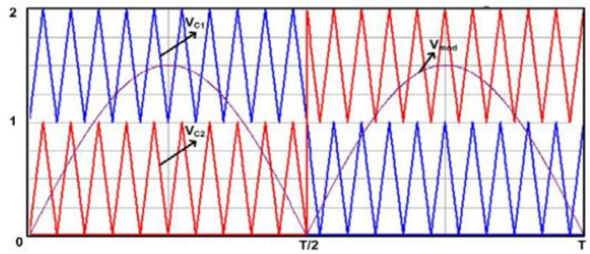

Fig.3 Hybrid Multicarrier Modulation

5. THIRD HARMONIC INJECTION (THI)

Fig.4 shows the (THIPWM) in which triplen harmonic voltage is added to each of the carrier waveforms. The method takes the instantaneous average of the maximum and minimum of the three reference voltages (Va, Vb, Vc) and subtracts the value from each of the individual reference voltages to obtain the modulation waveforms.

$$Voffset = \frac{\{\max(Va,Vb,Vc) + \min(Va,Vb,Vc)\}}{2} \quad (3)$$

$$VaTHI = Va - Voffset \quad (4)$$

$$VbTHI = Vb - Voffset \quad (5)$$

$$VcTHI = Vc - Voffset \quad (6)$$

It is appropriate only for a three phase three wire system due to the zero sequence modification made by this particular PWM technique. However it allows increase in the modulation index by 15% before the occurrence of an over modulation or pulse dropping [7].

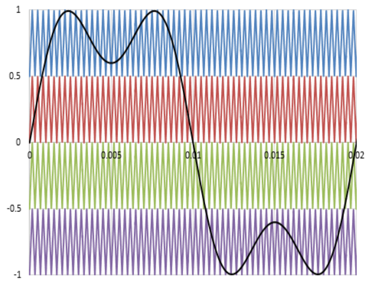

Fig: 4 Third Harmonic Injection

6. LOOKUP TABLE METHOD (LTM)

The proposed technique is based on space vector modulation (SVM) which is suitable for variable-frequency drive application. In this method the desired output can be obtained by formulating the data as per our requirements. In this way the switching instant are predicted such that the generated reference waveforms result in reduced CMV. Substantial reduction in the total harmonic distortion (THD) is possible in this technique. In SVM 3 phase quantities can be transformed to an equivalent of 2 phase quantity either in synchronously rotating frame or stationary frame with constant amplitude vector rotating at a constant frequency obtained from their three phase sinusoidal forms given below [8]-[10].

$$V_a = V_m \sin \omega t \quad (7)$$

$$V_b = V_m \sin(\omega t - 2\pi/3) \quad (8)$$

$$V_c = V_m \sin(\omega t - 4\pi/3) \quad (9)$$

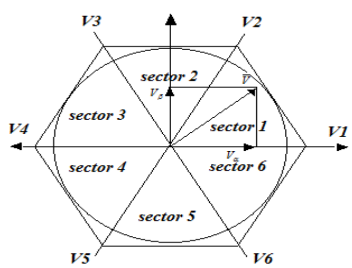

Fig: 5 Representation of rotating vector in complex plane

Representation of rotating vector in a complex plane is shown in Fig. 5 and Fig. 6 shows the carrier waveforms for LTM. The Space vector representation of 3 phase quantity is given as

$$\bar{V}* = V_\alpha + jV_\beta = \frac{2}{3}(V_a + aV_b + a^2V_c) \quad (10)$$

Where $a = e^{j\frac{2\pi}{3}}$ (11)

By solving equation (10) using (11) V_α, V_β is obtained as shown below.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (12)$$

Space vector in dq plane is given as [9]-[10].

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (13)$$

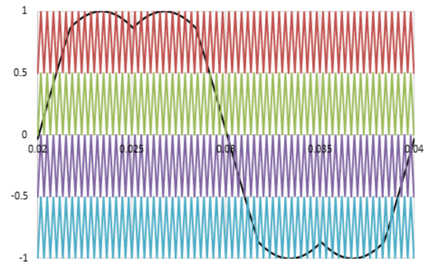

Fig: 6 Space Vector Modulation

In this paper SVM is implemented using the Lookup Table Method where the Switching sequence for each sector is considered as shown in Table 1.

Table-1 Switching Sequence of SVM

Sector	Switching Sequence
1	[1 1 0.5; 0 1 0.5; 0 0 0.5]
2	[1 0 0.5; 1 1 0.5; 0 0 0.5]
3	[0 0 0.5; 1 1 0.5; 0 1 0.5]
4	[0 0 0.5; 1 0 0.5; 1 1 0.5]
5	[0 1 0.5; 0 0 0.5; 1 1 0.5]
6	[1 1 0.5; 0 0 0.5; 1 0 0.5]

7. HARDWARE

Matlab Simulink is interfaced with Arduino for generating PWM signal using ATMEGA328P-PU. The analog signal from the Matlab Simulink is fed to the ATMEGA328P-PU and the controller produces the digital gated pulses which is fed to the Power circuit (Cascaded Mutilevel Inverter). The Fig.7 shows the outline for the hardware implementation. The hardware setup is shown in Fig. 8 Input voltage per bridge is 19 volts and load is 50 ohms (resistive load). 5 level inverter involves 2 bridges that produces 38 volts as output voltage.

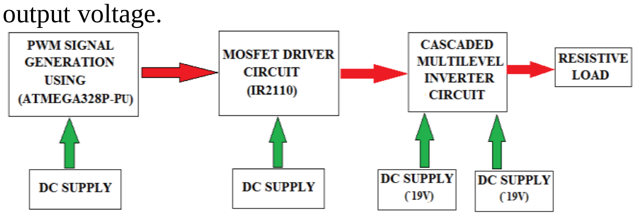

Fig.7 Outline of the hardware setup

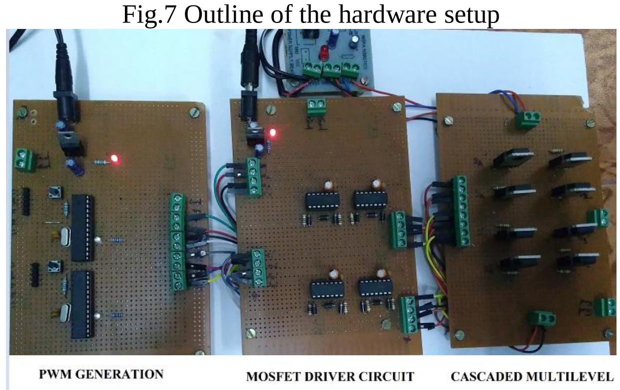

Fig. 8 Hardware setup for HMCM with Lookup Table Method

8. SIMULATION RESULTS

Fig. 9, Fig. 10 and Fig. 11 Shows the output voltages vs time, output current vs time and leakage current vs time waveforms for HMCM using Lookup Table Method. In this paper 5 level cascaded H-Bridge multilevel inverter is considered. Here two

H-bridge inverters are cascaded to get a 5 level output waveform. 19V DC is given as the input to each H-bridge inverter. Simulation parameters include resistor R=50ohms, capacitor L=0.1mH.

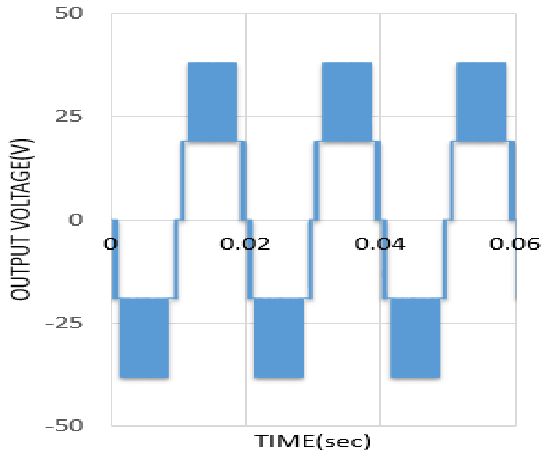

Fig.9 Output Voltage Vs Time

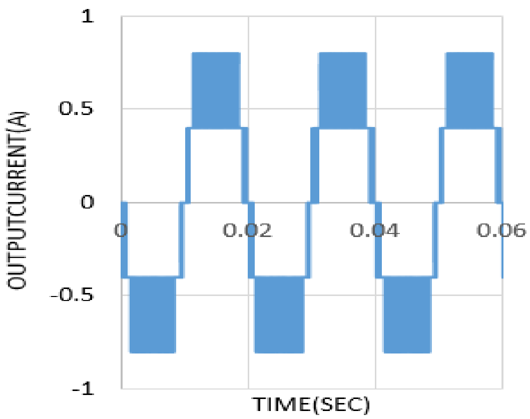

Fig. 10 Output Current Vs Time

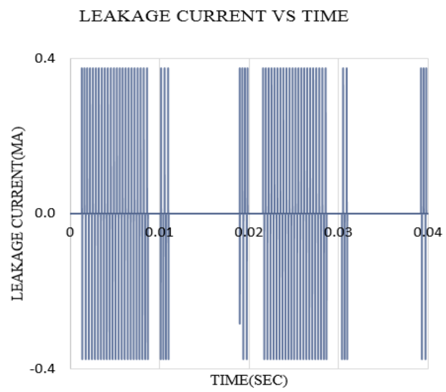

Fig.11 Leakage Current Vs Time

9. HARDWARE RESULTS

Fig.12, Fig.13, Fig.14 shows the output voltage vs time, output current vs time and leakage current vs time for the hardware setup of HMCMLTM.

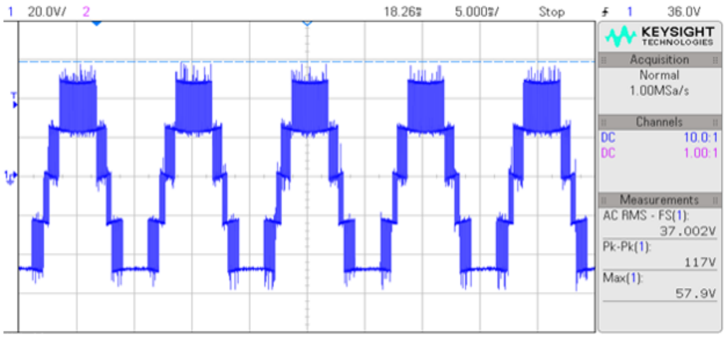

Fig.12 Output Voltage Vs Time

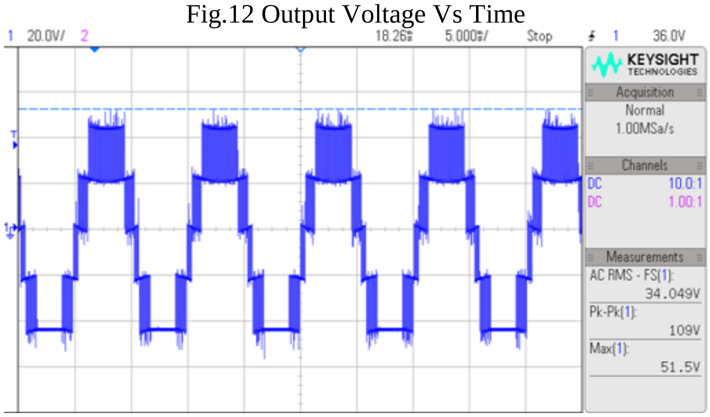

Fig.13 Output Current Vs Time

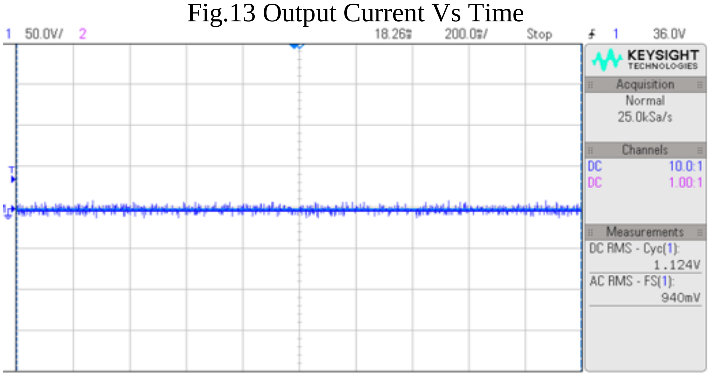

Fig.14 Leakage Current Vs Time

10. COMPARARIVE ANALYSIS

Table 2 shows the comparative analysis of HMCM, HMCMTHI, HMCMLTM. Among these three methods HMCMLTM has less leakage current. Table 3 shows the comparative analysis of simulation and hardware results of HMCMLTM.

Table -2. Comparison Of HMCM, HMCMTHI And HMCMLTM

INDICES	HMCM	HMCM USING THI	HMCM USING LTM
Output voltage(v)	38.26	37.96	37.29
Output Current (A)	0.7652	0.7592	0.7457
Leakage current(mA)	0.2984	0.2979	0.2937
CMV(V)	9.53	9.475	9.325

Table-3 Comparative Analysis Between Hardware and Simulation Results For HMCMLTM

INDICES	HMCM USING LTM (SIMULATION RESULTS)	HMCM USING LTM (HARDWARE RESULTS)
Output voltage(v)	37.29	37.00
Output Current (A)	0.7457	0.68
Leakage current(mA)	0.2937	0.28
CMV(V)	9.325	8.0

11. CONCLUSION

The hardware setup for HMCM with Lookup Table Method was built and the output voltage, output current and the leakage current was compared with the simulation results. The leakage current in the hardware setup is validated with to simulation results (0.2 mA range). HMCMLTM gives better results when compared with HMCM, HMCMTHI in case of simulation .But the hardware results and simulation results for HMCMLTM gives closer values. Thus it is inferred that HMCMLTM gives reduced leakage current compared to other method.

12. REFERENCES

[1] Ebrahim Babaei, “ A New General Topology for Cascaded Multilevel Inverters With Reduced Number of Components Based on Developed H-Bridge” , IEEE Transactions Industrial Electronics, Vol. 61, No. 8, August 2014.

[2] E. Babaei and S. H. Hosseini, “New cascaded multilevel inverter topology with minimum Manage., vol. 50, no. 11, pp. 2761–2767, Nov. 2009.

[3] J.Rodriguez,J.Lai,And F.Z.Peng, “Multilevel Inverters: A Survey Of Topologies, Controls and Application” , IEEE Transactions On Industrial Electronics, Vol. 49, No. 4, August 2002.

[4] Fusheng Wang, Zhen Li, Hieu Thanh Do, and Dehui Zhang,“A Modified Phase Disposition Pulse Width Modulation to Suppress the Leakage Current for the Transformerless Cascaded H-Bridge Inverters”, IEEE Transactions On Industrial Electronics, Vol. PP, Issue 99, July 2017.

[5] G Sreedevi, I. Akhila, Ch Santosh Kumar, D Padmavathi, “ A Simplified Approach to Hardware Implementation of Seven Level Cascaded Multilevel Inverter”, International Jounal of Electronics, Electrical and computational system(IJEECS), ISSN 2348-117X, Vol. 4, Issue5, May5.

[6] Rajasekar Selvamuthukumaran, Abhishek Garg, and Rajesh Gupta, “Hybrid Multilevel Modulation to Reduce Leakage Current In Transformerless Cascaded Multilevel Inverter For Photovoltaic Systems”, IEEE Transactions on Power Electronics, 0885-8993 © 2013 IEEE.

[7] R. Brindha1 , V. Ganapathy1 ,S. Apnapriya1 ,J. Venkataraman1,“Third Harmonics Injection Applied To Three Phase/Three Level/Three Switch Unidirectional PWM Rectifier”, International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 3, Special Issue 2, April 2014.

[8] R Gonzalez, J Lopez, P Sanchis and L Marroyo, “ Transformerless Inverter for Single- Phase Photovoltaic Systems”,IEEE Trans. On Power Electron, Vol.22 No. 2, PP.693-697, March 2007.

[9] A M Hava and E Un, “ A High- Performance PWM Alogorithm for Commom-Mode- Voltage Reduction in Three-Phase Voltage Source Inverters”,IEEE Trans on Power Electron, Vol. 26, No.7,PP. 1998-2008, Jully 2011.

[10] K.Zhou and D Wang, “Relationship between Space-Vector Modulation and Three Phase Carrier-Based PWM: A Comprehensive analysis”, IEEE Trans. Ind. Electron, Vol. 49, No.1, PP. 186-196, Jan 2002.